

Docket No.: 42P12661C

IN THE CLAIMS:

The status of the claims is as follows:

1. (Currently Amended) A semiconductor package comprising:
a semiconductor die having an integrated circuit (IC);
a substrate having a die side coupled to the IC, the substrate including a plurality of die-side contact pads, a plurality of socket-side contact pads and a base having a plurality of traces and vias interconnecting the die-side contact pads and the socket-side contact pads; and
a plurality of multi-signal bus bars coupled in a substantially perpendicular orientation to a socket side of the substrate, the bus bars to enable input/output (I/O) signals to be transported between the substrate and a socket.
2. (Previously presented) The package of claim 1 wherein at least one of the multi-signal bus bars includes:
a first dielectric member;
an electrically conductive reference member coupled to a first surface of the first dielectric member, the reference member defining a current path for a reference signal; and
a first plurality of electrically conductive I/O members coupled to a second surface of the first dielectric member through a dielectric layer, the first I/O members to define current paths for a corresponding first plurality of I/O signals.
3. (Previously presented) The package of claim 2 wherein the first I/O members have a predetermined spacing, the first I/O members being electrically isolated from one another.

Docket No.: 42P12661C

4. (Original) The package of claim 3 further including a dielectric layer disposed between the first dielectric member and the first I/O members.

5. (Original) The package of claim 2 wherein the I/O members have a current carrying capability that is above a predetermined current threshold.

6. (Original) The package of claim 2 wherein the I/O and reference members are bonded to the dielectric member with an adhesive material.

7. (Previously presented) The package of claim 2 wherein the bus bar is to have an inductance that is controlled to a predetermined inductance threshold for an operating frequency of the IC.

8. (Previously presented) The package of claim 2 wherein the multi-signal bus bar further includes:

a second dielectric member having a first surface coupled to the reference member, the dielectric members being positioned on opposite sides of the reference member; and

a second plurality of electrically conductive I/O members coupled to a second surface of the second dielectric member, the second I/O members to define current paths for a corresponding second plurality of I/O signals.

9. (Previously presented) The package of claim 2 wherein the reference member is to provide a current path for a reference voltage.

Docket No.: 42P12661C

10. (Previously presented) The package of claim 2 wherein the reference member is to provide a current path for a reference ground.

11. (Previously presented) The package of claim 1 wherein the multi-signal bus bars have a substantially planar overall geometry.

12. (Canceled).

13. (Original) The package of claim 1 wherein the IC is a computer processor.

14. (Previously presented) A multi-signal bus bar comprising:

a dielectric member;

an electrically conductive reference member coupled to a first surface of the dielectric member, the reference member defining a current path for a reference signal; and

a plurality of electrically conductive I/O members coupled to a second surface of the dielectric member, the I/O members to define current paths for a corresponding plurality of I/O signals, the bus bar having a substantially planar overall geometry.

15. (Previously presented) The bus bar of claim 14 wherein the I/O members have a predetermined spacing, the I/O members being electrically isolated from one another.

16. (Previously presented) The bus bar of claim 14 further including a dielectric layer disposed between the dielectric member and the I/O members.

Docket No.: 42P12661C

17. (Original) The bus bar of claim 14 wherein the I/O members have a current carrying capability that is above a predetermined current threshold.

18. (Original) The bus bar of claim 14 wherein the members are bonded to the dielectric member with an adhesive material.

19. (Original) The bus bar of claim 14 wherein the bus bar is to have an inductance that is controlled to a predetermined inductance threshold.

20. (Previously presented) A semiconductor package comprising:
a semiconductor die having a computer processor;
a plurality of die-side contact pads;
a plurality of board-side contact pads;
a substrate base having a plurality of traces and vias interconnecting the die-side contact pads and the board-side contact pads.

a first dielectric member;
an electrically conductive reference member coupled to a first surface of the dielectric member, the reference member to define a current path for a reference signal;

a first plurality of electrically conductive I/O members coupled to a second surface of the first dielectric member through a first dielectric layer, the first I/O members to define current paths for a corresponding first plurality of I/O signals;

a second dielectric member having a first surface coupled to the reference member, the dielectric members being positioned on opposite sides of the reference member; and

a second plurality of electrically conductive I/O members coupled to a second surface of the second dielectric member, the second I/O members to define current paths for a

Docket No.: 42P12661C

corresponding second plurality of I/O signals the dielectric members and the I/O members defining a multi-signal bus bar having a substantial planar overall geometry.

21. (Previously presented) The package of claim 20 wherein the I/O members have a predetermined spacing, the I/O members being electrically isolated from one another.

22. (Previously presented) The package of claim 21 wherein the second plurality of electrically conductive I/O members is coupled to the second surface of the second dielectric member through a second dielectric layer.

23. (Previously presented) A method, the method comprising:
coupling an electrically conductive reference member to a first surface of a dielectric member, the reference member defining a current path for a reference voltage signal; and
coupling a plurality of electrically conductive I/O members to a second surface of the dielectric member to obtain a multi-signal bus bar having a substantially planar overall geometry, the I/O members defining current paths for a corresponding plurality of I/O signals.

24. (Previously presented) The method of claim 23 further including coupling the I/O members to the second surface at a predetermined spacing, the I/O members being electrically isolated from one another.

25. (Previously presented) The method of claim 23 further including bonding the I/O and reference members to the dielectric member with an adhesive material.